International Journal of Electrical and Electronics Engineering (IJEEE)
ISSN(P): 2278-9944; ISSN(E): 2278-9952
Vol. 5, Issue 4, Jun - Jul 2016, 33-42

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

REDUCE ENERGY CONSUMPTION IN WI-FI MAC LAYER TRANSMITTER & RECEIVER BY USING EXTENDED VHDL MODELING

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ABSTRACT

Mobility and portability is the major advantages that IEEE 802.11 wireless networks offer over their traditional counter- parts, i.e. wired Ethernet networks. However, when nodes are mobile or portable units, power consumption becomes a primary issue since terminals are usually battery driven.

The wireless local area network, WLAN is dominated by IEEE 802.11 standard. It becomes one of the main focuses of the WLAN research. Now most of the ongoing research projects are simulation based as their actual hardware implementation is not cost effective. The main cores of the IEEE 802.1 lb standard are the CSMA\CA, Physical and MAC layers. But only MAC layer for transmitter and receiver are modeled in this paper using the VHDL modeling with the reducing of power consumption.

The VHDL (Very High Speed Hardware Description Language) is defined in IEEE as a tool of creation of electronics system because it supports development, verification, synthesis and testing of hardware design, the communication of hardware design data and the maintenance, modification and procurement of hardware. It is a common language for electronics design and development prototyping The main purpose of the IEEE 802.11 standards are to provide wireless connectivity to devices that require a faster installation, such as Laptops, PDA's or generally mobile devices inside a WLAN.

Using proposed algorithm, we develop a case study and provide interesting indications to minimize the power consumption of IEEE 802.11 terminals.

KEYWORDS: WLAN, IEEE 802.11, VHDL, Wi-Fi Mac Layer, FPGA

INTRODUCTION TO IEEE 802.11

Due to technology advancement in the 21St Century, wireless Communication had been most popular choices of communication. More and more people are turning to wireless due to the convenience of mobility. An 802.11 LAN is based on a cellular architecture where the system is subdivided in to cells, where each cell [called Basic Service Set or BSS] is controlled by a Base Station [called Access point, or in short AP].

In IEEE 802.11 networks, channel access is ruled by the CSMA/CA (Carrier-Sense Multiple Access with Collision Avoidance) medium access control algorithm.

Compared to a pure random access protocol, CSMA/CA reduces the collision probability by forcing each station to sense the channel before transmitting. Such strategy is enforced by the use of a classical random back off scheme. Channel sensing, however, is an energy–demanding process, and previous research [1–3] ascribed the high energy cost of

communication in IEEE802.11 Networks to the collision avoidance technique.

Our network model is a cluster of IEEE 802.11 terminals using the Distributed Coordination Function (DCF), which is the native adhoc mode used, in practice, by all commercial wireless devices. Such terminals share the same radio channel, i.e. there is no hidden or exposed node [4; 5]. We further assume that the cluster is under heavy traffic conditions, so that at each instant we have exactly *active* packets: under this assumption, in fact, each node in the cluster is either performing the exponential back off procedure or transmitting a packet. In the following we make a standard hypothesis [4] and assume that the probability that a transmitted packet collides at a given time slot is a constant, Independent of the transmission history of the cluster.

The problem, in modeling the energy consumption of such an ad–hoc network is that, due to the channel sensing procedure, nodes are constantly either transmitting, or listening to the channel. This implies that even all receiving operations should be accounted in order to quantify the energy consumption of a transmitting station. Also, it is known from previous work [1; 3] that the energy cost to receive is close to the cost of transmission.

WI-FI MAC LAYER TRANSMITTER AND RECEIVER

Overview of MAC Layer

The 802.11 protocol covers the MAC and physical layer, the standard currently defines a single MAC which interacts with three physical layers [all of them running at 1 and 2Mbits\sec]i.e. Frequency Hopping Spread Spectrum in the2.4GHz band, Direct Sequence Spread Spectrum in the 2.4GHz band and Infrared [3].

Beyond the standard functionality usually performed by MAC layers, the 802.11 MAC performs other functions that are typically related to upper layer protocols, such as Fragmentation, Packet retransmissions acknowledgements. The MAC layer defines two access methods, the Distribution Coordination Function [DCF] and Point Coordination Function [PCF] [3].

MAC layer acts as an intermediate stage between Data Link Layer and Physical Layer. Its primary responsibility is to provide a reliable mechanism for exchanging transacting packets [Data, Control and Management] on the communication channel through physical layer [RF layer]. MAC layer performs the following transmit functions i) Generation of various MAC frames [Data, Control, and Management] (ii) Generation of 16 bit HEC for Header and 32 bit CRC for payload data iii) CRC and HEC generation for payload &Header respectively iv) FIFO buffer interface for transmitter v) Serializing the data using byte to bit converter vi) MAC transmitter controller state machine implementation. Medium Access control [MAC] layer performs function like i) On transmission, assemble data in to a frame with address and error detection fields ii) On reception, disassemble frame and perform address recognition and error detection iii) Govern access to the LAN transmission medium Physical layer performs |functions like. i) Encoding/decoding of signals ii) I Preamble generation/ removal [for Synchronization].iii) Bit transmission I reception iv) Includes specifications of the transmission medium [4].

CONTRIBUTION AND RELATED WORK

Wi-Fi Wireless Fidelity [802.11 family of standards] for LAN Wi-Fi is designed for local area networks, which are private, local cable systems run at very high speeds. Wi-Fi achieves greater than l/O MB its/ Sec throughput for a user in many circumstances. Currently Wi-Fi carries more user data than any other wireless technology. Evolution is to go

further, faster and at lower power consumption [2]Upstart wireless LAN [WLAN] technologies under the 802.11 (Wi-Fi) umbrella have leapfrogged towards cellular and other efforts edging towards broad band wireless [such as 802.16! WiMAX] and have led to the first wide spread, commercially successful broadband wireless access technology. In fact, Wi-Fi is a runaway A success around the globe.

Block Diagram of Transmitter and Reciever

As discussed earlier, the transmitter block is divided in to five parts as shown in fig 4 and only two blocks are considered for VHDL simulation. These are Payload Data Storage block & Data Processing block.

A. Payload Data Storage Block

This is divided into two modules i.e. FIFO module & Data length counter module. These modules are F.1 discussed as shown below.

(i) FIFO Module FIFO Module is shown in Figure 1. It contains the data to be transmitted. It acts as the synchronizing tool i.e. the data are entered at high rate but it is retrieved at the slower rate. Here, we have taken 32x8bits of data storage. Here, the first incoming data goes out first. It acts on two clocks i.e. Sys Clk and Byte Clk, on their rising edge and when the FIFO is enabled the input data is retrieved. The Full and Empty signals shows the state of the FIFO.

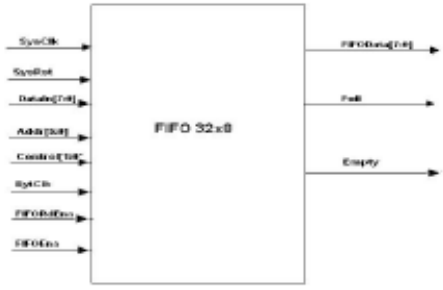
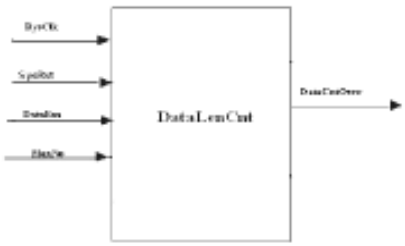


Figure 1: Fifo Module

(ii) ***Data length counter module: -*** Figure 2 shows Data length counter module. This module acts as a counter. It simply accepts a Max Number and counts the data being transmitted. When the number of the data is equal to the Max Number then the Data Count Over signal is turned high. It acts at every rising.



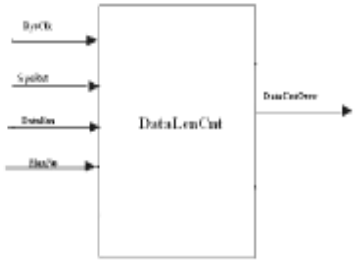


Figure 2: Data Length Counter Module

B. Data Processing Block

It is divided into three modules i.e, Serializer, HEC and CRC and they are discussed in details as shown below:

(i) Serializer Module: - Figure 3 a shows serializer Module. It is basically the parallel input and serial out put device. Various data selected at the multiplexer are serially obtained. It occurs at every rising edge of the clock and when the serial enable is high. The output bit is designated as SBit. When all the output bits are over, then the End of Conversion i.e. EOC goes high.

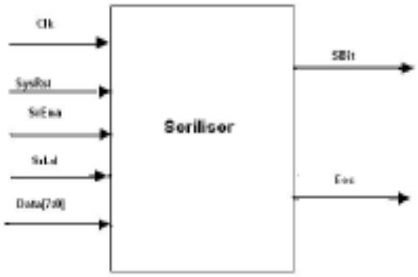


Figure 3: Serializer Module

(ii) HEC Module:- Figure. 4 shows HEC Module. This module produces the Head Error Check bits. It is the 16-bit error check bit. The HEC is calculated when the HRC Cal En a is high and when the TxEna is high then the HEC data is transmitted along with the PLCP Header Bits.

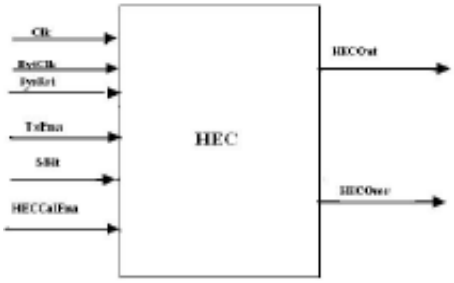


Figure 4: HEC Module

(iii) **CRC Module**:- Figure 5 shows CRC module. The 32-bit Cyclic Redundancy Check. When the Tx Ena signal is high, then the CRC data is given out and when the CRCCI Ena is high, then the CRC is calculated. CRC Over is high when the transmission of the data is over. This module helps in error free transmission of the data with proper reliability.

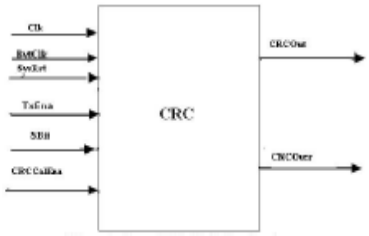


Figure 5: CRC Module

VHDL Modeling of Wi-Fi Mac Layer for Transmitter and Reciever

There are two types of widely used hardware description languages i.e. Verilog HDL with C-language like syntax, easy to learn and another is VHDL which follows the structure of ADA programming language. Verilog and VHDL each have about 50% share of the commercial user base [8]. VHDL is acronym for VHSIC i.e. very large scale integrated circuit hardware description language. It was standardized by IEEE. VHDL is used for synthesis construct and implement a design on silicon. VHDL is used for simulation to imitate real world scenarios for verification [9]. Due to high computational complexity of WLAN systems and the capabilities of state-of-the-art microprocessor s, an implementation based solely in microprocessors would require a large number of components and would be cost inefficient FPGAs with their spatial / parallel computation style can significantly accelerate complex parts of WLANs and improve the efficiency of discrete components implementations [I0].The design has been synthesized using FPGA. This device belongs to the virtex -E group of FPGAs from xilinx. Two types of FPGAs (Field Programmable Logic Array) are available i.e.i) Reprogrammable (SRAM) based) from Xilinx, Altera, Lattice and Atmel ii) One- time Programmable (OTP) from Actel, Quick logic.

FPGAs are reasonably cheap, with short design cycle and are reprogrammable. They are more flexible than PLDs and more compact than MSI/SSI. FPGAs have evolved to meet new application demands with features like i) Newer devices incorporate entire CPUs i.e. Xilinx Virtex II pro has 1-4 power PC CPUs ii) Have carry chains to have a better support for multi-bit operations iii) Have integrated memories, such as block RAMs in the devices we use iv) Have specialized units, such as Multipliers to implement functions that are Slow/ inefficient in CLBs [Configurable Logic Blocks] [6]FPGA enables high performance due to the following factors i)Tailoring to desired bit-width (ii) Ease of applying varying sample rates (iii) Flexibility of parallel execution of basic functions due to uniform architectural resources [7] Here, two modules of Wi-Fi MAC layer transmitter are chosen and implemented on an FPGA device. The details of simulation are shown in Table 1.

Table 1: Details of Simulation

Property Name	Value
Device Family	VirtexE
Device	xcv300e
Package	fg456
Speed Grade	-8
Top-Level Module Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	Modelsim
Generated Simulation Language	VHDL

Proposed Energy Minimization Algorithm

Begin

1. For each task τ_i^j arriving during a period

   Do,

   a. Compute Ta_i^j using

$Ta_i^j = \min\left(\left((rel_h^x - rel_i^j) + slack_i^j\right), d_i\right)$ -------(1)

   b. If $(Ta_i^j \geq R_i(m_{i,} k_{i,} Sa_i)$

      i. Compute the energy requirement $\in_{new1}$

      ii. Go to step 1. C.

      Else

      i. Initialize w_L with the speed index of sa_i

      While

      ii. $\left((Ta_i^j < R_i(m_{i,}\ k_{i,} S_{wL})\right) AND\ w_L << N)$

      Do

      1. $w_L = w_L + 1$

      Repeat

      iii. Compute the energy requirement $\in_{new2}$

      iv. Select the higher priority job τ_h^x having minimum laxity,

      $$slack_i^j = \min(laxity)$$

      v. Initialize w_h with the speed index of Sa_h

      vi. $w_h = w_h + 1$

      vii. Compute Ta_i^j using equation—(1)

      viii. While $\left((Ta_i^j < R_i(m_{i,}\ k_{i,} Sa_i)\right)$

      Do

      1. Go to step 1

      ix. Compute the energy requirement $\in_{new3}$

   c. Find minimum energy configuration min $(\in_{new1}, \in_{new2,} \in_{new3})$ and assign.

   d. Update the schedule.

   Repeat

   END

SIMULATIONS RESULTS

The payload data storage and data processing block consists of total of five different individual modules i.e. FIFO. Data length counters modules and Serializer, HEC, CRC modules respectively all these modules are simulated using modelsim and simulation results are shown in figure 7.8.9.10.11.

A. Simulation Results of Fifo Module

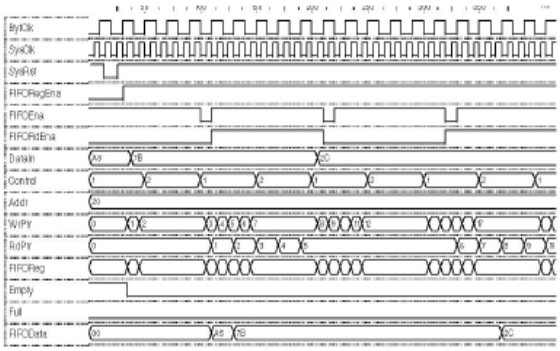


Figure 6: Simulation Indicates Enabling of FIFO of the Raising Edge of Two Clocks Sysclk and Byteclk

B. Simulation Results of Data Length Counter

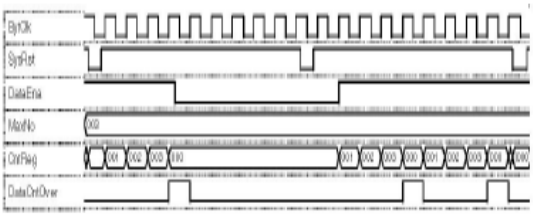


Figure 7: Simulation Indicate That, When the No .of Data is Equal to the Maximum Number, then the Data CNT over Signal Goes High

C. Simulation Waveforms Serializer Module

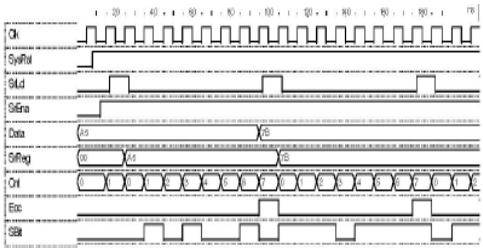


Figure 8: Simulation Indicates the End of Output Bits, EOC Goes High

D. Simulation Results of HEC Module

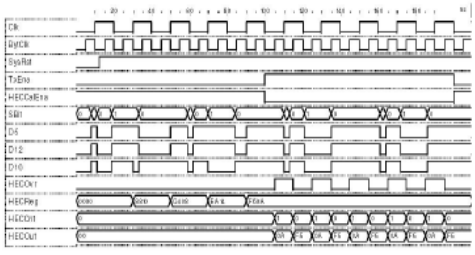


Figure 9: Simulation Indicates that When the T*ENA is High, HEC Data is Transmitted along the PLCP Header Bits

E. Simulation Results of CRC Module

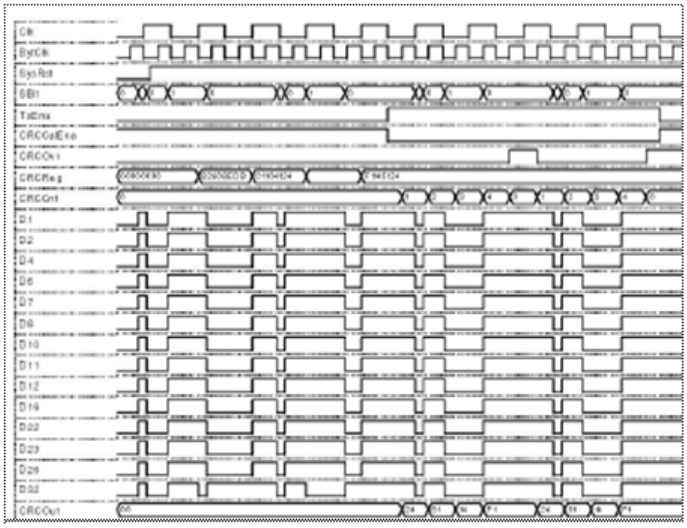


Figure 10: Simulation Indicate at the End of Transmission of the Data, CRC Over Goes High

F .Simulation of Proposed Algoritham

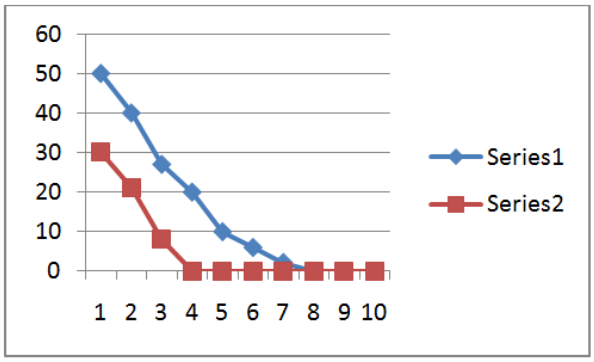


Figure 11: Result of Energy Consumption Algorithm

CONCLUSIONS AND FUTURE WORK

Various individual modules of Wi-Fi Transmitter have been designed, verified functionally using VHDL simulator, synthesized by the synthesis tool .This design of the Wi-Fi transmitter is capable of transmitting the frame formats. The formats include all 802.11 frames i.e. MAC frame, RTS frame , CTS frame and ACK frame. The transmitter is also capable of generating error checking codes like HEC and CRC. It can handle variable data transfer. And By the use proposed energy aware algorithm we reduce the energy consumption in Wi-Fi MAC Layer.

REFERENCES

1. W. L. Pang, K. W. Chew, F. Choong, E. S. Teoh, "VHDL Modeling of the IEEE802.1 lb DCF MAC", Procedings of the 6th WSEAS nternational Conference on Instrumentation, Measurment Circuits and systems, Hangzhou, China, April 15 -17,2007.
2. Broadband wireless Access, Institution of Engineering and Technology Seminar, 6th Dec 2006, London, UK
3. Pabolo Brenner, "A Technical tutorial on theIEE802.11 Protocol"

4. Shambhu Upadhyaya, “Wireless Network Security, “Lecture 5, University at Buffalo, the State University of Newyork
5. Sebastien Roy, “The Design of an FPGA Based MIMO Transceiver for Wi - Fi, "DSP Magazine, May2006
6. Prof. David Brooks, "Computer Science 141Computing Hardware "fall 2007, Harvard University.
7. Introduction to DSP Design flow, 2006 Xilinx, Inc
8. Janak. H. Patel, Introduction to VHDL 1 and 2, Deptof Electrical and Computer Engineering, University of Illinois at urbana - campaign.
9. Ahmed Abu-Hajar, Digital Design Using VHDLD igitavid, Inc, San Jose, CA
10. K. Masselos, N. S. Voros. "Implementation of of wireless Communications system on FPGA-Based platforms", EURASIP Journal on embedded systems, volume 2007, article ID 12192.